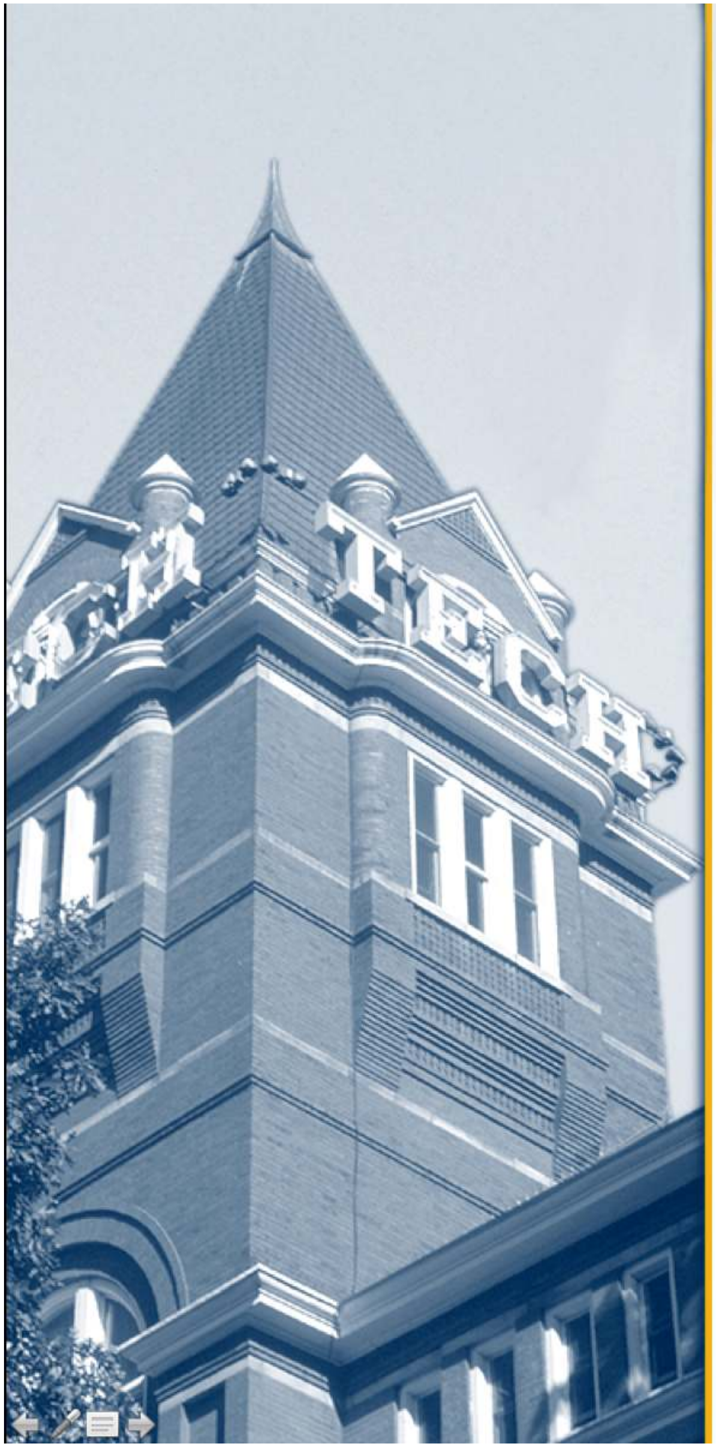
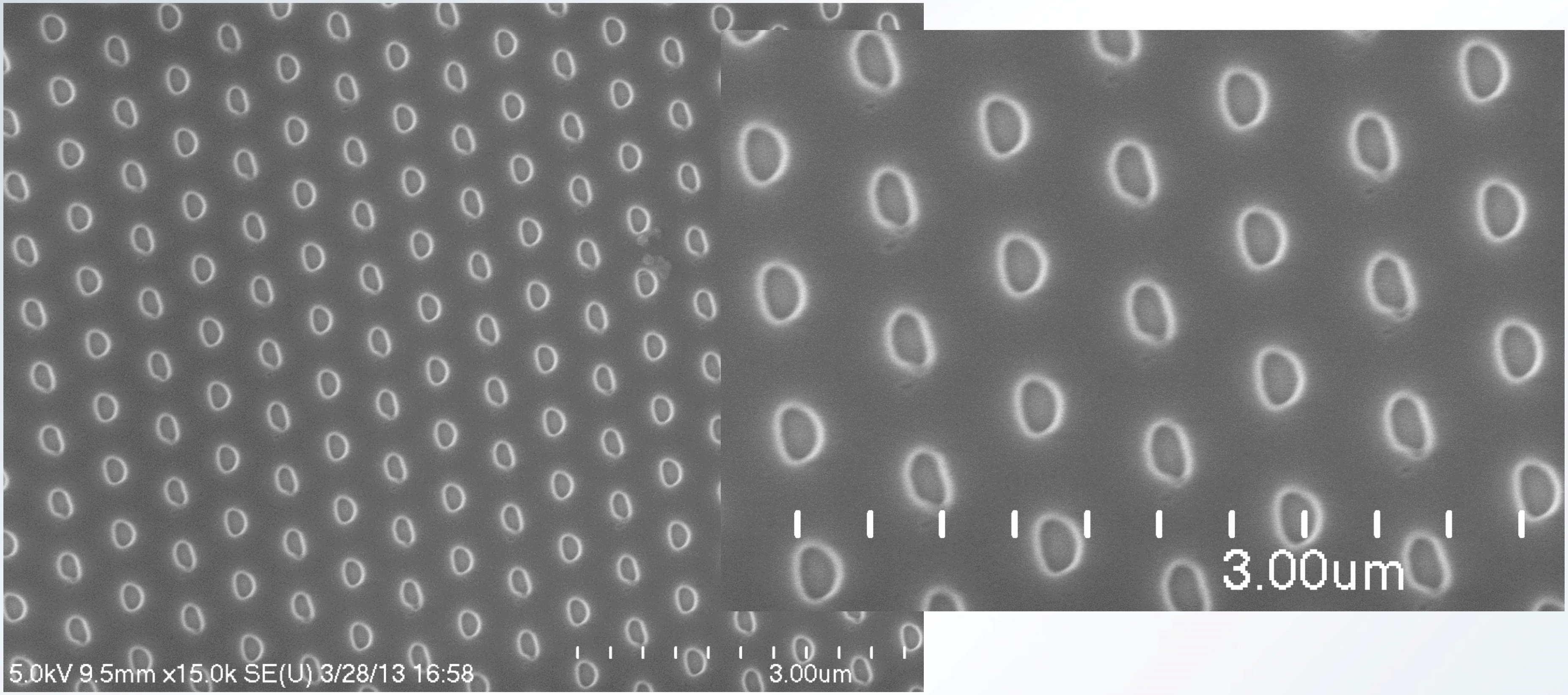


InSb etch development update

Devin Brown

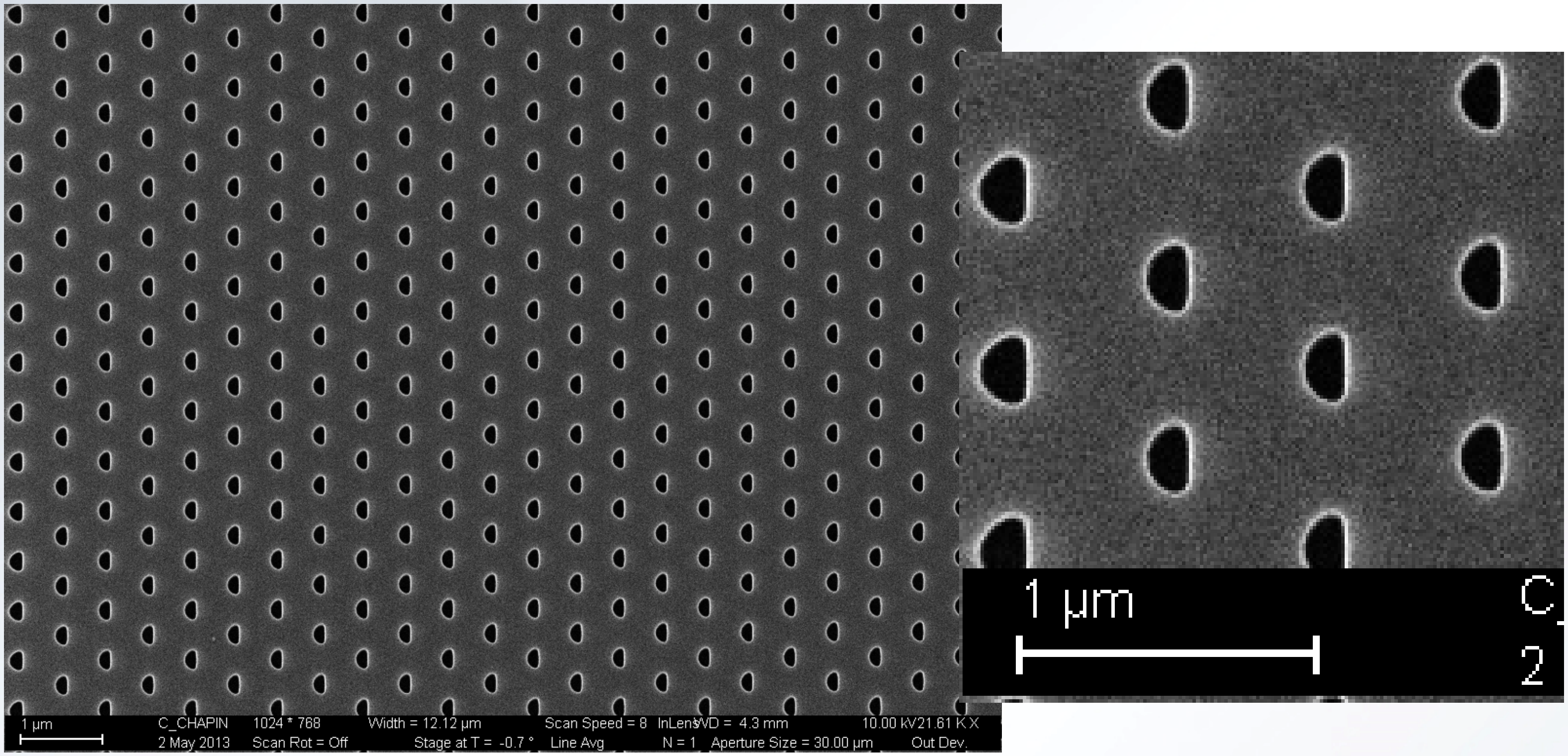
2/21/2014

EBL pattern definition in resist at 2 nA



- pattern in ZEP520 resist on InSb
- initially tried 2 nA beam current as this is our default setting
- semi-circles are not well formed (above)
- CAD definition, semi-circles, radius = 120 nm, hexagonal array pitch = 600 nm

EBL pattern definition in resist at 600 pA



- pattern in ZEP520 resist on InSb
- lowering beam current to 600 pA from 2 nA decreases beam diameter and improves resolution
- pattern quality is better
- CAD definition, semi-circles, radius = 120 nm, hexagonal array pitch = 600 nm

Georgia Tech

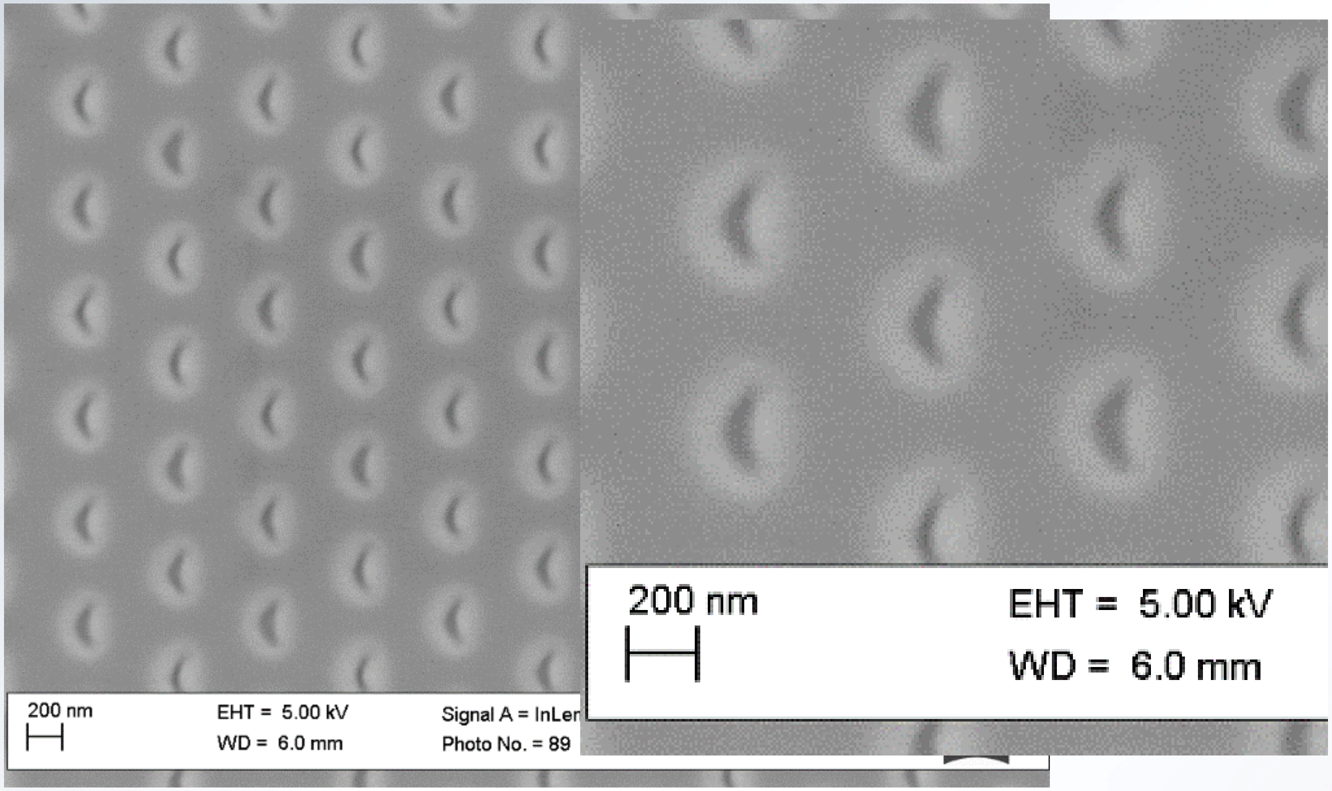
InSb ICP etching in literature

- 4 main papers on InSb ICP etching in literature
  - Diniz, et. al. 1998, "Inductively coupled plasma etching of In-based compound semiconductors in CH4/H2/Ar"
  - Hahn, et. al. 1999, "Effect of inert gas additive species on Cl high density plasma etching of compound semiconductors Part II. InP, InSb, InGaP and InGaAs"
  - Hahn, et. al. 2000, "Inductively Coupled Plasma Etching in ICl- and IBr-Based Chemistries. Part II: InP, InSb, InGaP, and InGaAs"
  - Zhang, et. al. 2009, "Inductively coupled plasma-reactive ion etching of InSb using CH4/H2 /Ar plasma"

InSb ICP etching in literature

- in general, two chemistries reported
  - Cl/Ar, where $InCl_x$ is the volatile product
  - CH_4/H_2, where SbH_3 is the volatile product
- most papers report that InSb etching in general produces high surface roughness (< 20 nm RMS) and may only be appropriate for through/via etching
- however Zhang, et. al. reports low roughness with CH_4/H_2 and RIE like conditions

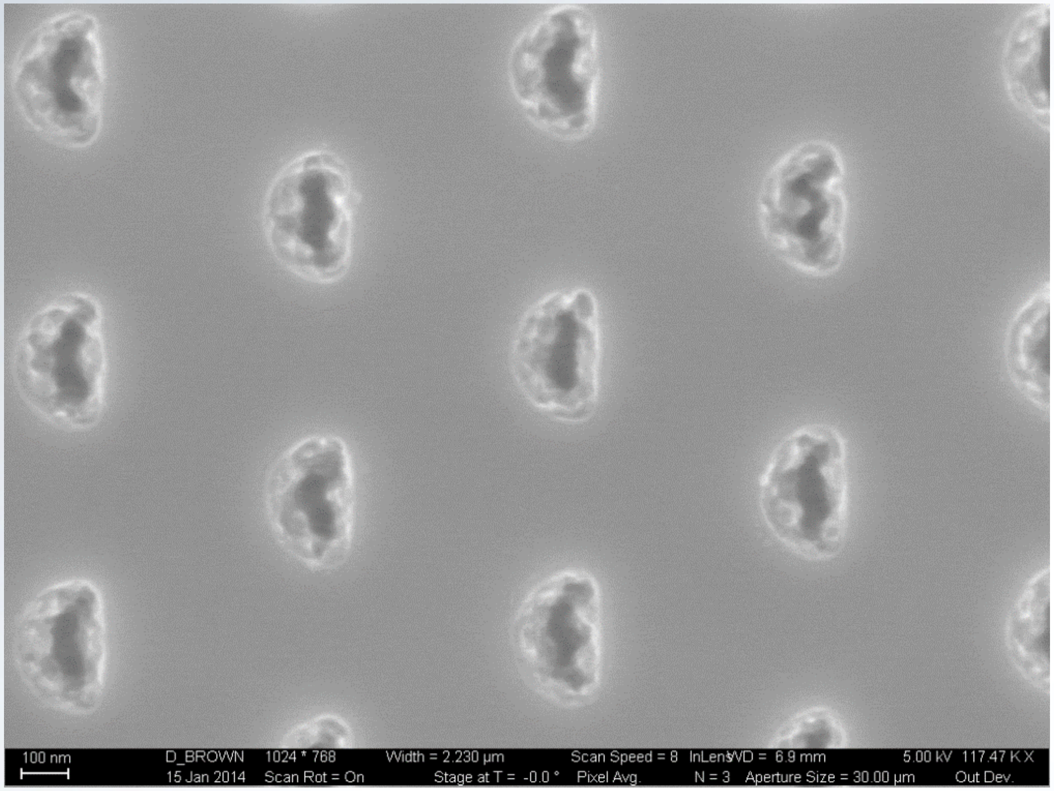
attempt with Cl/Ar



Plasma Therm ICP
recipe = TJB_INSB
press = 5 mTorr
Cl2 = 20 sccm
H2 = 15 sccm
Ar = 5 sccm
RF2 coil = 600 W
RF1 RIE = 200 W

- initially tried an existing Cl recipe for InSb
- result was not good, semi circles turned into crescents and etch was very shallow

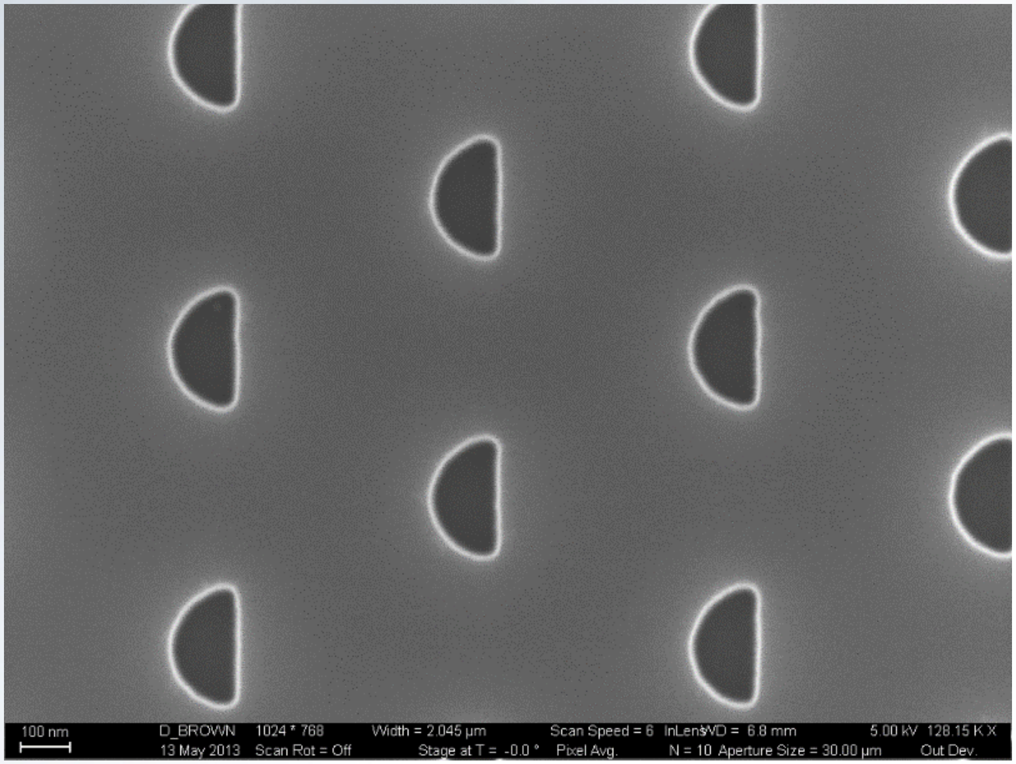
attempt with CH_4/H_2



tool = STS SOE
recipe = DKB_INSB
Ar = 5 sccm
CH_4 = 15 sccm
H_2 = 50 sccm
ICP = 600 W
RIE = 150 W
press = 7 mTorr

- attempted one of the promising conditions from Zhang, 2009
- however, etch result pretty rough for 120 nm features
- Zhang paper only shows ~5 um features, perhaps not representative for nanoscale

etching of Silicon as reference



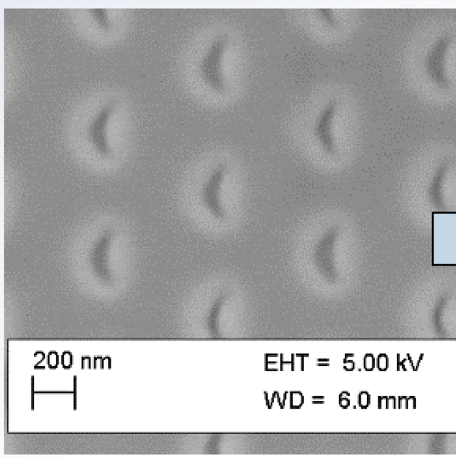
tool = Plasma Therm ICP, left chamber
recipe = DKB_SI
16 sccm Cl2
4 sccm Ar
press = 5 mTorr
50 W RIE
200 W coil

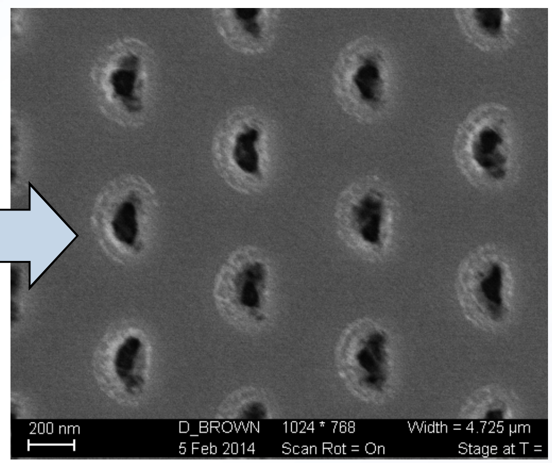
- above is the etch result with the same CAD pattern and EBL on *silicon* (post resist strip) with a known good etch recipe
- because silicon etch result is good, we know that EBL lithography is good, and bad result in InSb is due to etch recipe

second Cl2 attempt

first recipe attempt
Plasma Therm ICP
recipe = TJB_INSB
press = 5 mTorr
Cl_2 = 20 sccm
H_2 = 15 sccm
Ar = 5 sccm
RF2 coil = 600 W
RF1 RIE = 200 W

second recipe attempt
Plasma Therm ICP
recipe = DKB_SI
press = 5 mTorr
Cl_2 = 16 sccm
~~no H2~~
Ar = 4 sccm
RF2 coil = 200 W
RF1 RIE = 50 W





- second recipe attempt drops H_2 (Hahn, 1999 does not use H_2, but attempts Ar, He, and Xe), H_2 may be hindering Cl and producing CH by-products as it reacts with resist
- lowering coil and RIE/platen powers to more RIE like conditions (reported by Zhang, 2009 to have lower roughness)
- result with second recipe does look better/deeper than first Cl_2 attempt, but there is roughness

second CH4 attempt

first recipe attempt
tool = STS SOE
recipe = DKB_INSB
press = 7 mTorr
CH_4 = 15 sccm
H_2 = 50 sccm
Ar = 5 sccm
ICP = 600 W
RIE = 150 W

second recipe attempt
tool = STS SOE
recipe = DKB_INSB (#2)
press = 7 mTorr
CH_4 = 15 sccm
H_2 = 50 sccm
Ar = 5 sccm
ICP = 600 W
RIE = 50 W

- try lowering RIE power from 150 W to 50 W per data from Zhang, 2009
- however, result still looks rough, actually worse so