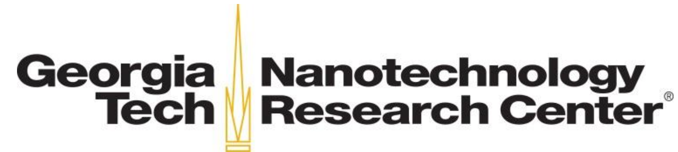


JBX-9300FS Process Monitor 58 Results

April 25, 2012

Process Conditions

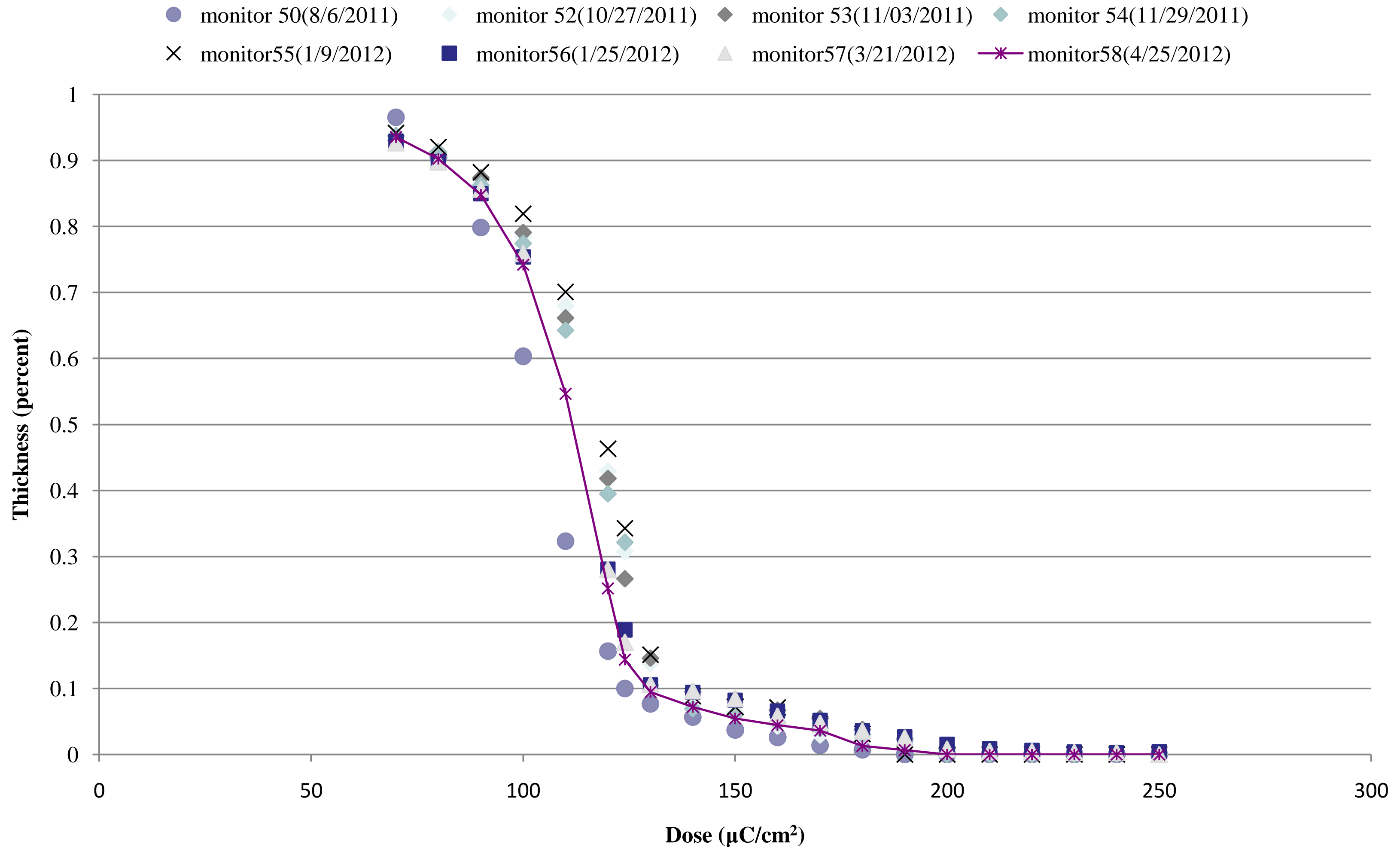
Substrate:
- 4” silicon wafer cleaved into 1”x1” piece, then spun

Coat:
- ZEP520A resist
- 5000 RPM, 2500 RPM / sec, 60sec
- 180°C hot plate bake for 2 minutes
- Thickness: 314 nm (measured on the Nanospec reflectometer)

Expose:
- 2 nA current, 100 kV accelerating voltage, 8 nm shot pitch
- Dose varied for 100 nm line features

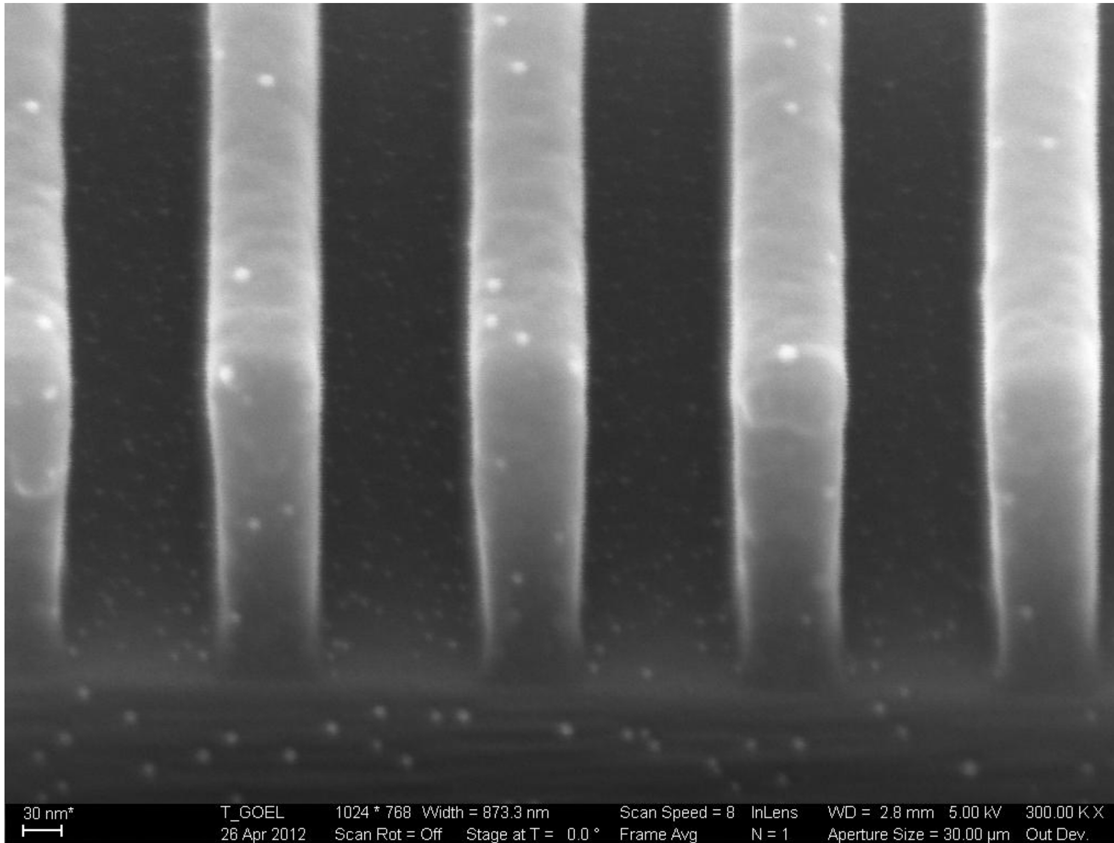
Develop:
- Amyl acetate immersion for 2 minutes
- Isopropanol immersion for 30 seconds
- N_2 blow dry

Dose to Clear



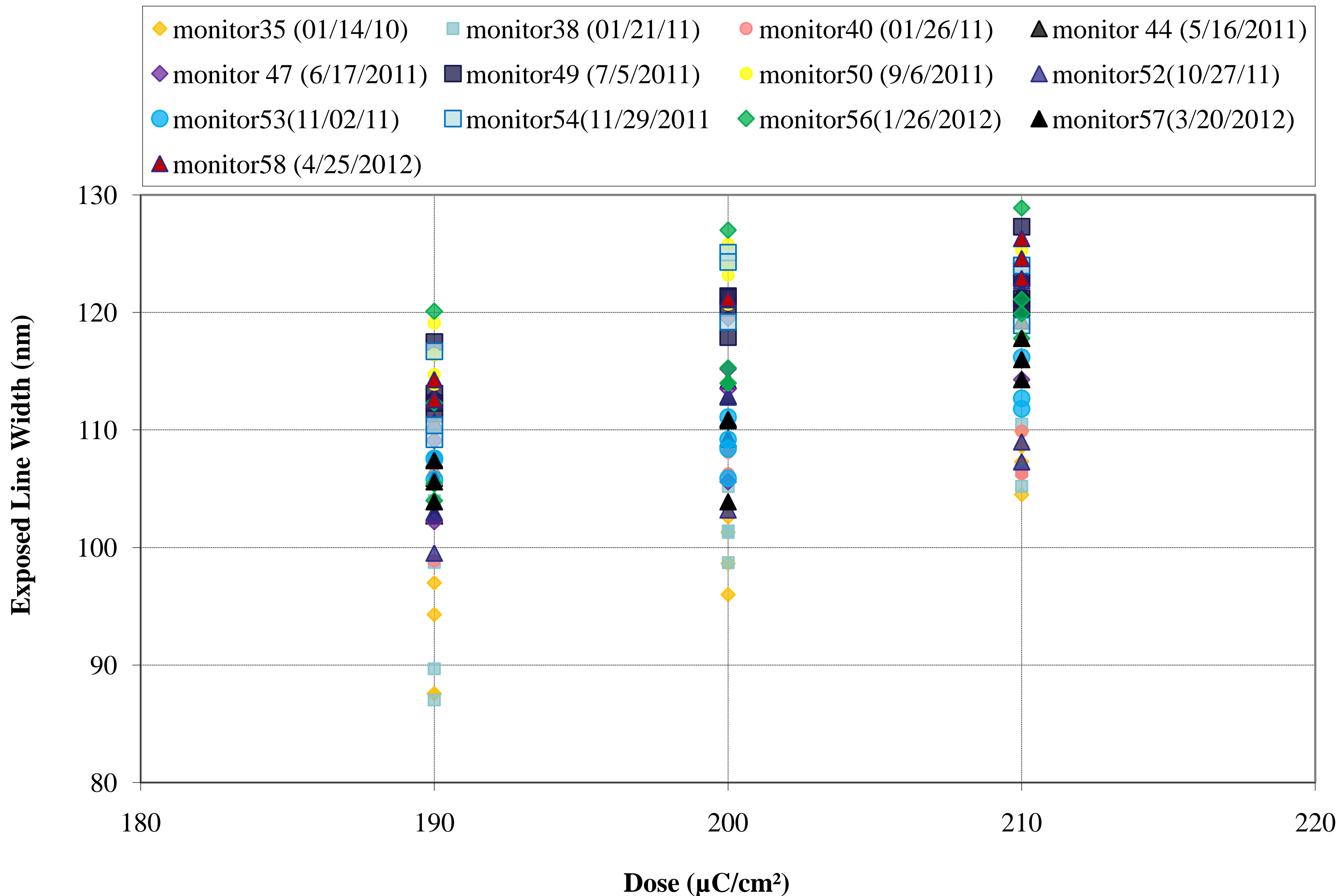
- Thickness measured on exposed 75 μm squares with the Nanospec reflectometer
- reflectometer recipe = 019 ZEP on Silicon (10X)

SEM image of 100 nm line and space



- CAD file, line and space drawn at 100 nm
- line and space grating occupies a 50 um x 3 mm area
- dose = 210 μC/cm²

Line Width Comparison for 100nm Line and Space

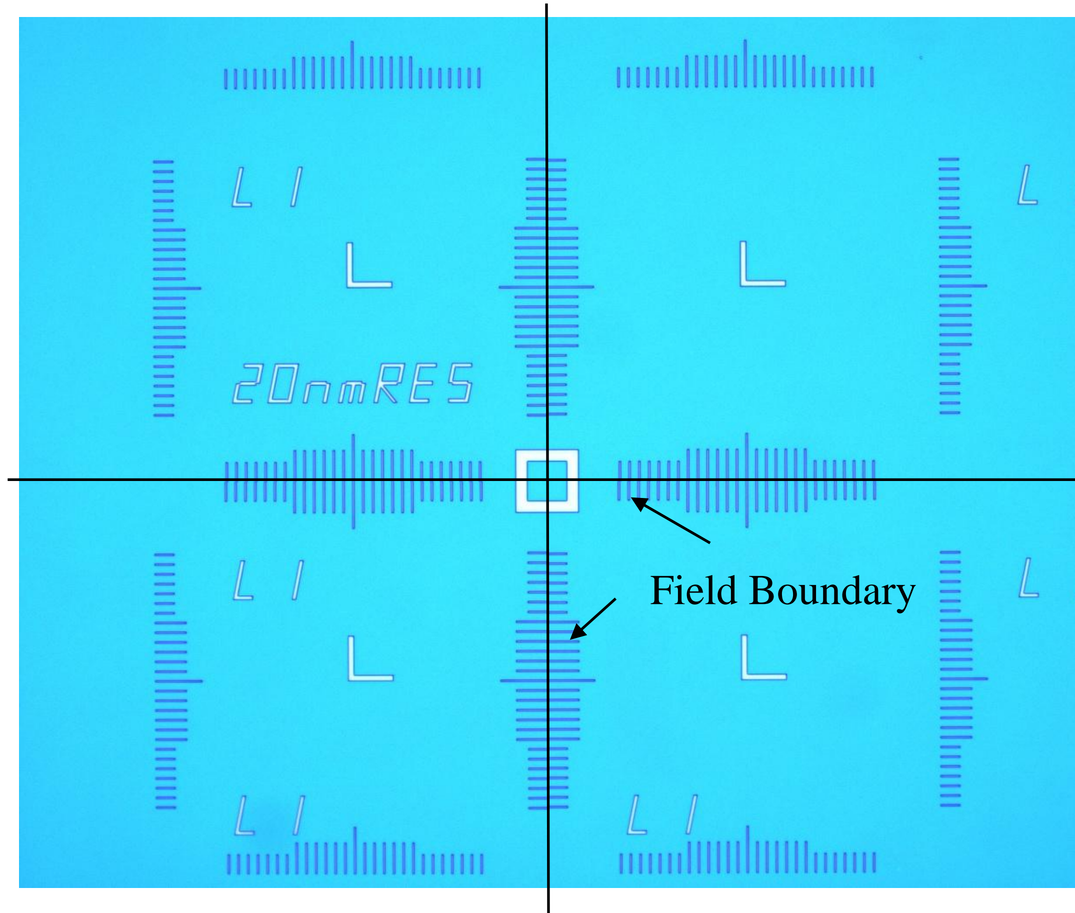


Monitor 58 lines appear a little larger than normal, but fall in an acceptable range.

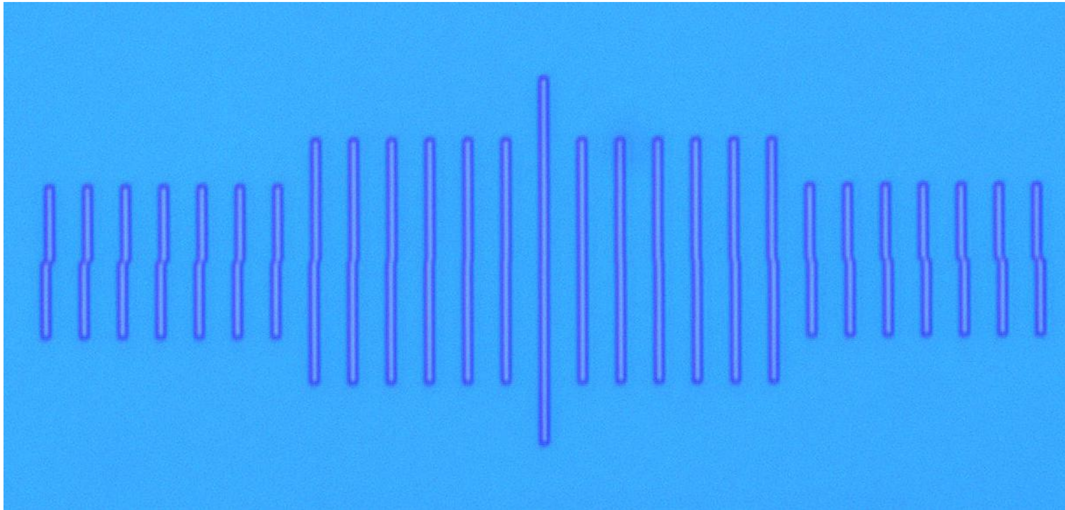
Georgia Tech Nanotechnology Research Center

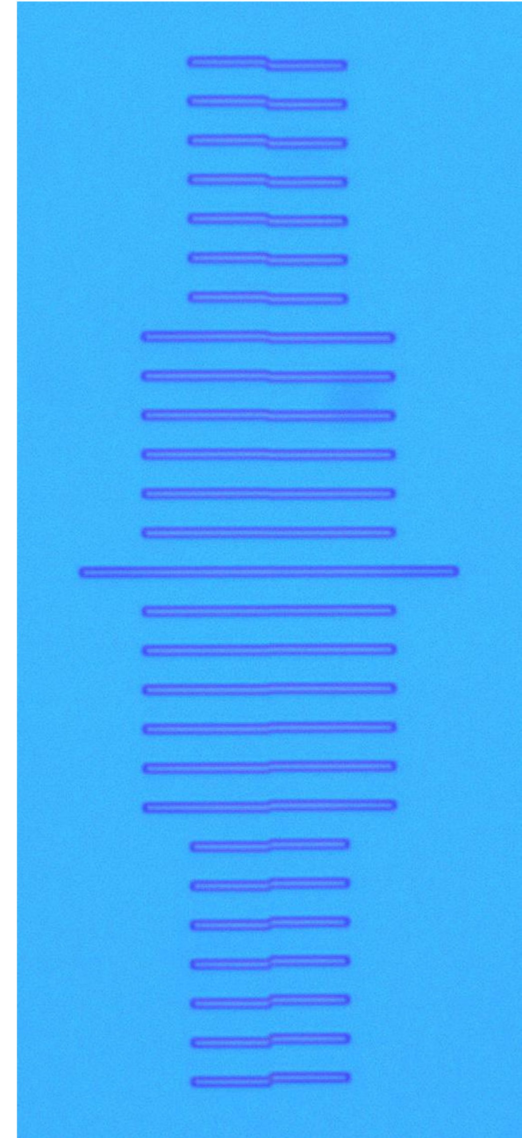
vernier pattern for field stitching alignment

The center lines should not have stitching error; they should be straight. If another line is straight then there is a stitching error of n*20nm, where “n” is the number of lines off of center.



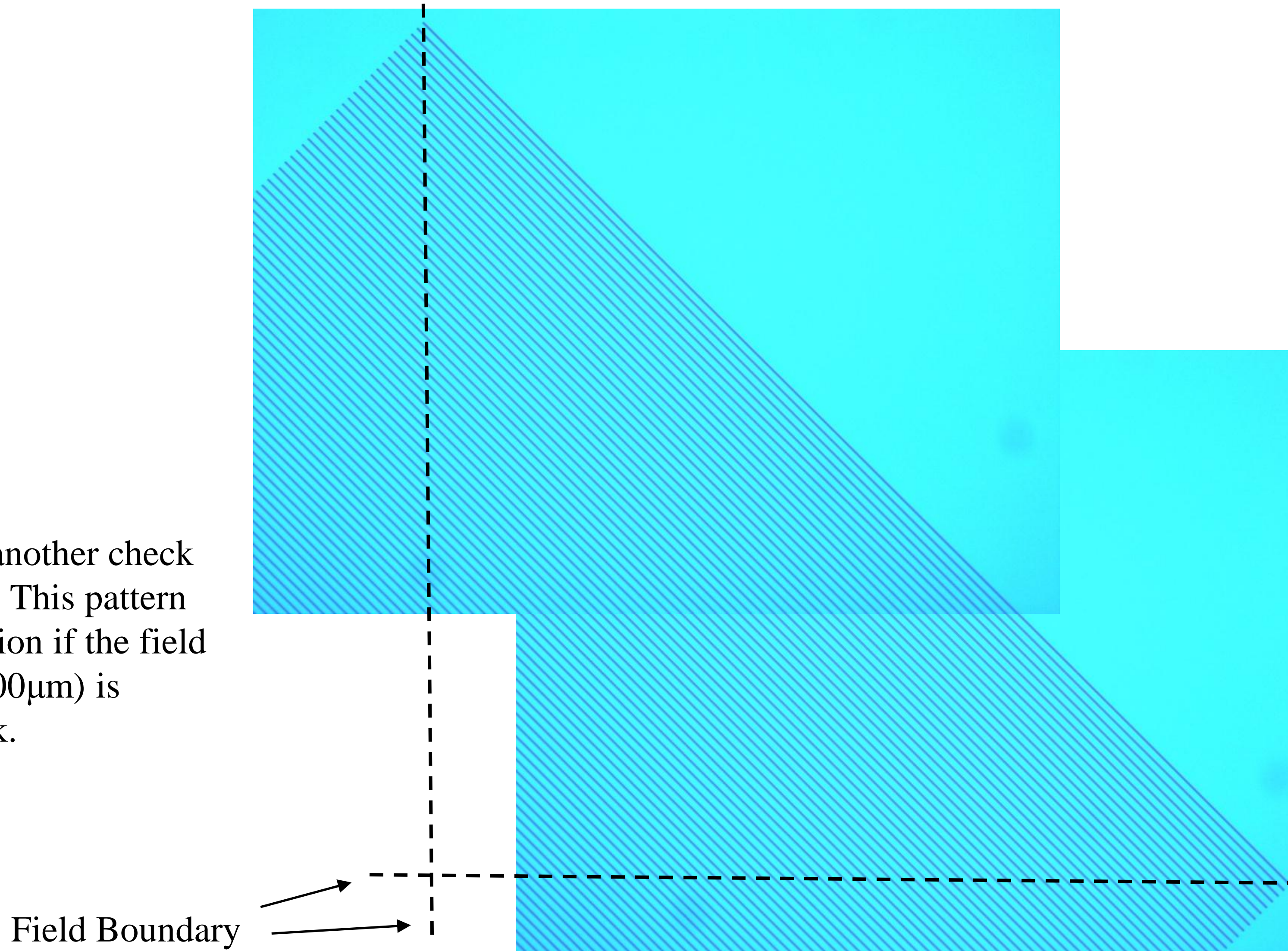
Vernier pattern for field stitching alignment





After examining the field boundary of the Vernier pattern, there appears to be less than 20nm of stitching error well within spec.

Diagonal Square Pattern to Check for Stitching



Diagonal pattern another check for field-stitching. This pattern also shows distortion if the field size (500µm by 500µm) is enlarged or shrunk.